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EXAMINER	
TABONE JR, JOHN J	
ART UNIT	**PAPER NUMBER**
2133	4

DATE MAILED: 04/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)	
	10/023,537	RUTTEN, IVO WILHELMUS JOHAOOES MARIE	
	Examiner	Art Unit	
	John J Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-18 have been examined.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 4 rejected is under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The claim is not supported by the specification, but merely refers to a copending application "CHIP-MOUNTED CONTACT SPRINGS", Ser. No. _____ filed Nov. 8, 2001 for Ivo Rutten, Attorney Docket US018180, which teaches a contact technology that is particularly well suited for use in this invention, and is incorporated by reference herein. (See page 4, ¶ 36). This copending application teaches the bonding of a segment of bonding wire to two adjacent points, the specification of the instant application does not. This renders this claim non-enabled because the details are not included in the specification.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 5, 11, 15, 17, and 18:

The use of the word "therefrom" in these claims is unclear and indefinite. It is not clear what is generating or providing "therefrom" test signals or responses. It can be any of the preceding limitations. Applicant is respectfully requested to clearly define what is generating or providing the test signals or responses and remove "therefrom" from these claims.

Claims 2-4, 6-10, 12-14, 16:

These claims are rejected because they depend on claims 1 and 11 and contain the same problems of indefiniteness.

Claim 4:

The limitation "bonded to two substantially adjacent points" is indefinite and, furthermore, is not supported and defined by the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 5, 8-11, and 14-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Arkin et al. (US-6028439).

Claim 1 and 9:

Arkin teaches a modular integrated circuit tester 10 (ATE) that performs a sequence of tests on one or more (plurality) and differing types (i.e. digital logic , memory, analog/digital) of integrated circuit devices under test (DUT) 12. Tester 10 includes a set of tester modules 14(1)-(3) (programmable integrated circuit), each of which conducts all test activities at a corresponding set of terminals of DUT 12 during each test. (Col. 4, lines 44-50; col. 16, lines 19-23). Arkin also teaches tester 10 also includes a host computer 16 (computer) connected to tester modules 14(1)-14(3) through a conventional network 18, suitably an Ethernet network including a conventional network hub 17 and serial network buses 19 (interface circuit). Arkin also discloses Host 16 (computer) receives input instructions (sequence of testing operations) from a user and forwards those instructions to modules 14 (programmable IC) via network 18 (interface circuit). (Col. 5, lines 5-16). Arkin further teaches tester 14(1) includes local microcontroller 30 (programmable integrated circuit) that communicates with host 16 (computer) through an Ethernet port 32 and Ethernet bus 19 (interface circuit). (Col. 7, lines 31-42).

Claim 11:

The limitation of "a programmable component" is rejected per claim 1. Arkin also teaches that integrated circuit tester includes a test head, a structure that provides the

physical contact between tester electronics and the IC (plurality of contact points). (Col. 2, lines 18-21).

Claim 17:

This claim is rejected per claim 1.

Claim 2:

Arkin teaches that integrated circuit tester includes a test head, a structure that provides the physical contact between tester electronics and the IC (plurality of contact points). (Col. 2, lines 18-21).

Claim 5:

Arkin teaches that upon the DUT passing all tests, the main program of one of the modules prompts the DUT to send a "DUT pass" message to the host 16 via the network 18 (ATE receives at least one test response from the DUT). (Col. 5, lines 63-67). Arkin also teaches host 16 (ATE) receives the test result data from the controllers (programmable IC) of the appropriate modules via network 18. Arkins further discloses any of modules 14(1)-14(3) (programmable IC) may respond to its local DUT_FAIL signal (receives a response signal from the DUT) by sending a "DUT fail" message to host 16 via network 18 telling it that DUT 12 is defective (communicates to the ATE). (Col. 6, lines 4-23).

Claim 8:

Arkin teaches that bandwidth limitations on the bus connecting the host to the tester boards provide a practical limit to the number of tester boards that the host can reprogram within a reasonable time between tests. (Col. 2, lines 52-55). Arkin also

teaches tester 10 also includes a host computer 16 connected to tester modules 14(1)-14(3) through a conventional network 18, suitably an Ethernet network (interface circuit) including a conventional network hub 17 and serial network buses 19 (first bandwidth). (Col. 5, lines 5-8). Arkin further discloses that during a digital logic test, activities of the various tester modules 14 are synchronized to a centrally generated master clock signal MCLK produced by a clock signal source 15 (second bandwidth). (Col. 4 61-64).

Claim 10:

Arkin teaches that FIG. 9 is a flow chart illustrating a START SYNC subroutine the main routine of FIG. 8 calls to synchronize operations of module 14(1) to other modules of tester 10 of FIG. 1. Arkin also teaches at step 100, local microcontroller 30 of FIG. 2 executes the setup instructions for the digital logic test. (Col. 14, lines 34-64).

Claim 14:

Arkin teaches tester channel 40(1) includes a pin electronics circuit 72 for supplying the test signal to the DUT terminal (communicates to the DUT) in response to a set of drive control signals (D, Z and VH) (test signals). Arkin further teaches tester channel 40(1) includes a formatter circuit 74 (components to configure the test signals) which receives the FSET data from pattern generator 20 and supplies the drive control signals D, Z and VH to pin electronics circuit 72. (Col. 11, lines 39-41, 55-57, 64-67).

Claim 15:

Arkin teaches host 16 (ATE) receives the test result data from the controllers (programmable component) of the appropriate modules via network 18. Arkins further discloses any of modules 14(1)-14(3) (programmable IC) may respond to its local

DUT_FAIL signal (receives a response signal from the DUT) by sending a "DUT fail" message to host 16 via network 18 telling it that DUT 12 is defective (communicates to the test system). (Col. 6, lines 4-23).

Claim 16:

Arkin teaches the tester channel 40(1) data CDAT pattern generator 46 (components configured to process response signal) of FIG. 2 supplies to each channel 40(1)-40(48) for each test cycle includes format set data (FSET), time set data (TSET), and reference data (PG). The FSET data references a particular drive or compare format the channel is to use during the cycle. Arkin further teaches a compare format defines how the channel determines the expected states of the output signal and how the channel compares the output signal to its expected states and produces the FAIL signal (response signal). (Col. 11, lines 16-38).

Claim 18:

Arkin teaches a modular integrated circuit tester 10 (ATE) that performs a sequence of tests on one or more (other devices-under-test) integrated circuit devices under test (DUT) 12 which also includes a set of tester modules 14(1)-(3) (programmable integrated circuit), each of which conducts all test activities at a corresponding set of terminals of DUT 12 during each test and can be expanded to include a larger number of tester modules (other programmable integrated circuits). (Col. 4, lines 44-53).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3, 4, 6, 7, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arkin et al. (US-6028439) in view of D'Souza (US-5323107).

Claim 3 and 12:

Arkin does not explicitly teach "the at least one point of contact includes a bonding pad", however, Arkin does teach that integrated circuit tester, which includes a set of tester modules 14(1)-(3) (programmable integrated circuit), includes a test head, a structure that provides the physical contact between tester electronics and the IC (contact points). (Col. 2, lines 18-21). D'Souza teaches an active probe card having integral test circuitry that applies test signals through probe pins to the integrated circuit input pads (bonding pads) and samples the test signal responses at the integrated circuit output pads. D'Souza also teaches the test circuitry is field programmable (programmable integrated circuit). (Col. 2, lines 42-57). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Arkins tester modules 14(1)-(3) (programmable integrated circuit) to be used as D'Souza's integral test circuitry on the active probe card. The artisan would be motivated to do so because it would enable Arkin's test modules to have direct contact to the DUT and facilitate testing of a plurality of devices.

Claim 4 and 13:

D'Souza teaches the test circuitry (programmable IC) applies test signals through the probe pins (resilient structure). (Col. 2, lines 47,48).

Claim 6:

Arkin does not explicitly teach "a probe card, upon which the programmable integrated circuit is mounted", however Arkin does teach that the tester modules 14 are connected to the terminals of DUT 12 to conduct all test activities. (Col. 4, lines 44-56). D'Souza teaches an active probe card having field programmable integral test circuitry that applies test signals through probe pins to the integrated circuit input pads (bonding pads) and samples the test signal responses at the integrated circuit output pads. (Col. 2, lines 42-57). D'Souza also suggests an Automatic Test Equipment (ATE) can be attached to the active probe card 500 through ports 502 to drive each of the probe pins 504. (Col. 6, lines 55-59, Fig. 9). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Arkins tester modules 14(1)-(3) (programmable integrated circuit) to be used as D'Souza's integral test circuitry on the active probe card. The artisan would be motivated to do so because it would enable Arkin's test modules to be coupled to the ATE and facilitate testing of a plurality of devices.

Claim 7:

Arkin teaches tester 10 performs a sequence of tests on one or more integrated circuit devices under test (DUT) 12 (plurality). Arkin also teaches although tester 10 is illustrated in FIG. 1 as including only three tester modules 14(1)-14(3), tester 10 may be

easily expanded to include a larger number of tester modules (plurality). (Col. 4, lines 44-53).

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arkin et al. (US-6028439).

Claim 9:

Arkin does not explicitly teach that "the device-under-test (DUT) includes a memory device", however, Arkin does teach the sequence of tests from the tester modules 14 include one or more digital logic tests. (Col. 2, lines 54, 55). Arkin suggests the ability of the microcontroller 30 to write to a memory, i.e. generates data and writes it to addressable memories (Col. 8, lines 65-67, col. 9, lines 1-4), loads data in RAM 66 (Col. 10, lines 57, 58), and stores the main program in RAM 34. Arkins also suggests the ability to address a memory while executing the main program starting at a RAM 34 address. (Col. 14, lines 39-45). It would have been obvious to one of ordinary skill in the art at the time the invention was made that the Arkin's tester modules 14 could be modified to test a memory DUT with the already existing circuitry. The artisan would be motivated to do so because Arkins already performs the writing and reading of internal memories with the tester module.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Arkin et al. (US-6,028,439)

Arkin teaches an IC tester 10 (programmable IC) for testing a DUT and a host computer 20. Claims 1, 11 and 17. Arkin also teaches memory test as well as digital logic test. Claim 9.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (703) 305-8915. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JJT

Albert DeCady
Primary Examiner